CLAIMS

What is claimed is:

1. A wireless Ethernet network device with active and low power modes, comprising:

a first voltage regulator that regulates supply voltage during the active mode and that is powered down during the low power mode;

a second voltage regulator that dissipates less power than said first voltage regulator and that regulates supply voltage during the low power mode;

a medium access controller (MAC) device that selects said first voltage regulator during the active mode and said second voltage regulator during the low power mode.

2. The wireless Ethernet network device of Claim 1 further comprising a baseband processor (BBP) that performs radio frequency mixing and that communicates with said MAC device.

3. The wireless Ethernet network device of Claim 2 wherein at least one of said first and second voltage regulators is located in said BBP.

4. The wireless Ethernet network device of Claim 2 further comprising a first phase locked loop (PLL) that generates a first clock signal for said BBP during the active mode.

5. The wireless Ethernet network device of Claim 4 wherein said first PLL is located in said BBP.

6. The wireless Ethernet network device of Claim 4 further comprising a crystal oscillator that outputs a timing signal to said first PLL during the active mode.

7. The wireless Ethernet network device of Claim 6 further comprising a radio frequency (RF) transceiver that transmits and receives wireless signals, that communicates with said BBP and that includes a second PLL that receives said timing signal from said crystal oscillator during the active mode and that generates a second clock signal for said RF transceiver.

8. The wireless Ethernet network device of Claim 7 further comprising a first oscillator that generates a third clock signal during the low power mode, wherein said first oscillator dissipates less power than said crystal oscillator.

9. The wireless Ethernet network device of Claim 1 wherein when said MAC device initiates the low power mode, said first voltage regulator is shut down.

10. The wireless Ethernet network device of Claim 7 wherein when said MAC device initiates the low power mode, said RF transceiver is shut down.

11. The wireless Ethernet network device of Claim 7 wherein when said MAC device initiates the low power mode, said first and second PLL are shut down.

12. The wireless Ethernet network device of Claim 7 wherein when said MAC device initiates the low power mode, said crystal oscillator is shut down.

13. The wireless Ethernet network device of Claim 8 wherein said MAC device includes a counter and wherein when said MAC device initiates the low power mode, said second voltage regulator powers said first oscillator and said counter.

14. The wireless Ethernet network device of Claim 13 wherein when said counter reaches a predetermined count, said MAC device powers up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL and said second PLL.

15. The wireless Ethernet network device of Claim 1 wherein said wireless Ethernet network device is operated in an infrastructure mode.

16. The wireless Ethernet network device of Claim 1 wherein said wireless Ethernet network device is operated in an ad hoc mode.

17. The wireless Ethernet network device of Claim 7 wherein said MAC device includes an external interface and wherein when said MAC device receives a wake up signal from a host via said external interface, said MAC device powers up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver and said first and second PLL.

18. The wireless Ethernet network device of Claim 6 wherein said MAC device powers down said first PLL before shutting down said first voltage regulator and said crystal oscillator.

19. The wireless Ethernet network device of Claim 6 wherein said crystal oscillator is an external crystal oscillator (XOSC).

20. The wireless Ethernet network device of Claim 6 wherein said crystal oscillator includes an external crystal and an amplifier that is integrated with one of said MAC device, said BBP, and said RF transceiver.

21. The wireless Ethernet network device of Claim 1 wherein said MAC device includes transmit and receive state machines and a transmit buffer and wherein said MAC device initiates said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle.

22. The wireless Ethernet network device of Claim 1 wherein said wireless Ethernet network device dissipates less than 2mW when in said low power mode.

23. The wireless Ethernet network device of Claim 6 further comprising a processor that communicates with said crystal oscillator and that calibrates said first oscillator using said timing signal from said crystal oscillator.

24. The wireless Ethernet network device of Claim 8 wherein said first oscillator is located in said BBP.

25. The wireless Ethernet network device of Claim 8 wherein at least two of said BBP, said first voltage regulator, said second voltage regulator, said RF transceiver, said MAC device, and said first PLL are implemented by a system on chip (SOC).

26. A baseband processor for a wireless Ethernet network device with active and low power modes, comprising:

a first voltage regulator that regulates supply voltage during the active mode and that is powered down during the low power mode; and

a second voltage regulator that dissipates less power than said first voltage regulator, and that regulates supply voltage during the low power mode.

27. The baseband processor of Claim 26 wherein said baseband processor receives a power mode select signal from a medium access controller.

28. The baseband processor of Claim 26 further comprising a first phase locked loop (PLL) that generates a first clock signal for said BBP during the active mode and that is powered down during the low power mode.

29. The baseband processor of Claim 28 wherein said first PLL receives a timing signal from a crystal oscillator during the active mode.

30. The baseband processor of Claim 29 further comprising a first oscillator that generates a second clock signal during the low power mode, wherein said first oscillator dissipates less power than the crystal oscillator.

31. A wireless Ethernet network device with active and low power modes, comprising:

first regulating means for regulating supply voltage during the active mode and that is powered down during the low power mode;

second regulating means, which dissipates less power than said first regulating means, for regulating supply voltage during the low power mode;

selecting means for selecting said first regulating means during the active mode and said second regulating means during the low power mode.

32. The wireless Ethernet network device of Claim 31 further comprising baseband (BB) processing means for performing radio frequency mixing and for communicating with said selecting means.

33. The wireless Ethernet network device of Claim 32 wherein at least one of said first and second regulating means is located in said BB processing means.

34. The wireless Ethernet network device of Claim 32 further comprising first phase locked loop (PLL) means for generating a first clock signal for said BB processing means during the active mode.

35. The wireless Ethernet network device of Claim 34 wherein said first PLL means is located in said BB processing means.

36. The wireless Ethernet network device of Claim 34 further comprising crystal oscillating means for outputting a timing signal to said first PLL means during the active mode.

37. The wireless Ethernet network device of Claim 36 further comprising radio frequency (RF) transceiver means for transmitting and receiving wireless signals, that communicates with said BB processing means and that includes a second PLL means for receiving said timing signal from said crystal oscillating means during the active mode and for generating a second clock signal for said RF transceiver means.

38. The wireless Ethernet network device of Claim 37 further comprising first oscillating means for generating a third clock signal during the low power mode, wherein said first oscillating means dissipates less power than said crystal oscillating means.

39. The wireless Ethernet network device of Claim 31 wherein when said selecting means initiates the low power mode, said first regulating means is shut down.

40. The wireless Ethernet network device of Claim 37 wherein when said selecting means initiates the low power mode, said RF transceiver means is shut down.

41. The wireless Ethernet network device of Claim 37 wherein when said selecting means initiates the low power mode, said first and second PLL means are shut down.

42. The wireless Ethernet network device of Claim 37 wherein when said selecting means initiates the low power mode, said crystal oscillating means is shut down.

43. The wireless Ethernet network device of Claim 38 wherein said selecting means includes counting means for counting and wherein when said selecting means initiates the low power mode, said second regulating means powers said first oscillating means and said counting means.

44. The wireless Ethernet network device of Claim 43 wherein when said counting means reaches a predetermined count, said selecting means powers up at least two of said crystal oscillating means, said first regulating means, said RF transceiver means, said first PLL means, said BB processing means and said second PLL means.

45. The wireless Ethernet network device of Claim 31 wherein said wireless Ethernet network device is operated in an infrastructure mode.

46. The wireless Ethernet network device of Claim 31 wherein said wireless Ethernet network device is operated in an ad hoc mode.

47. The wireless Ethernet network device of Claim 37 wherein said selecting means includes an external interface and wherein when said selecting means receives a wake up signal from a host via said external interface, said selecting means powers up at least two of said crystal oscillating means, said first regulating means, said RF transceiver means and said first and second PLL means.

48. The wireless Ethernet network device of Claim 36 wherein said selecting means powers down said first PLL means before shutting down said first regulating means and said crystal oscillating means.

49. The wireless Ethernet network device of Claim 36 wherein said crystal oscillating means is an external crystal oscillator (XOSC).

50. The wireless Ethernet network device of Claim 36 wherein said crystal oscillating means includes an external crystal and an amplifier that is integrated with one of said selecting means, said BB processing means, and said RF transceiver means.

51. The wireless Ethernet network device of Claim 31 wherein said selecting means includes transmit and receive state machines and a transmit buffer and wherein said selecting means initiates said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle.

52. The wireless Ethernet network device of Claim 31 wherein said wireless Ethernet network device dissipates less than 2mW when in said low power mode.

53. The wireless Ethernet network device of Claim 36 further comprising processing means that communicates with said crystal oscillating means for calibrating said first oscillating means using said timing signal from said crystal oscillating means.

54. The wireless Ethernet network device of Claim 38 wherein said first oscillating means is located in said BB processing means.

55. The wireless Ethernet network device of Claim 38 wherein at least two of said BB processing means, said first regulating means, said second regulating means, said RF transceiver means, said selecting means, and said first PLL means are implemented by a system on chip (SOC).

56. A baseband processor for a wireless Ethernet network device with active and low power modes, comprising:

first regulating means for regulating supply voltage during the active mode and that is powered down during the low power mode; and

second regulating means, which dissipates less power than said first regulating means, for regulating supply voltage during the low power mode.

57. The baseband processor of Claim 56 wherein said baseband processing device receives a power mode select signal from a medium access controller.

58. The baseband processor of Claim 56 further comprising first phase locked loop (PLL) means for generating a first clock signal for said processing means during the active mode and that is powered down during the low power mode.

59. The baseband processor of Claim 58 wherein said first PLL means receives a timing signal from a crystal oscillator during the active mode.

60. The baseband processor of Claim 59 further comprising a first oscillating means that generates a second clock signal during the low power mode, wherein said first oscillating means dissipates less power than the crystal oscillator.

61. A method for operating a wireless Ethernet network device with active and low power modes, comprising:

regulating supply voltage during the active mode using a first voltage regulator;

powering down said first voltage regulator during the low power mode; and

regulating supply voltage during the low power mode using a second voltage regulator, which dissipates less power than said first voltage regulator.

62. The method of Claim 61 further comprising performing radio frequency mixing using a baseband (BB) processor.

63. The method of Claim 62 further comprising locating at least one of said first and second voltage regulators in said BB processor.

64. The method of Claim 62 further comprising generating a first clock signal for said BB processor during the active mode using a first phase locked loop (PLL).

65. The method of Claim 64 wherein said first PLL is located in said BB processor.

66. The method of Claim 64 further comprising generating a timing signal for said first PLL using a crystal oscillator during the active mode.

67. The method of Claim 66 further comprising:

transmitting and receiving wireless signals using a radio frequency (RF) transceiver that includes a second PLL; and

receiving said timing signal from said crystal oscillator at said second PLL during the active mode and generating a second clock signal for said RF transceiver.

68. The method of Claim 67 further comprising generating a third clock signal during the low power mode using a first oscillator, wherein said first oscillator dissipates less power than said crystal oscillator.

69. The method of Claim 61 further comprising shutting down said first voltage regulator when the low power mode is initiated.

70. The method of Claim 67 further comprising shutting down said RF transceiver when the low power mode is initiated.

71. The method of Claim 67 further comprising shutting down said first and second PLL when the low power mode is initiated.

72. The method of Claim 67 further comprising shutting down said crystal oscillator when the low power mode is initiated.

73. The method of Claim 68 further comprising powering said first oscillator using said first voltage regulator and starting a counter when the low power mode is initiated.

74. The method of Claim 73 further comprising powering up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, said BB processor and said second PLL when said counter reaches a predetermined count.

75. The method of Claim 61 wherein said wireless Ethernet network device is operated in an infrastructure mode.

76. The method of Claim 61 wherein said wireless Ethernet network device is operated in an ad hoc mode.

77. The method of Claim 67 further comprising powering up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, and second PLL when a wake up signal from a host is received.

78. The method of Claim 66 further comprising powering down said first PLL before shutting down said first voltage regulator and said crystal oscillator.

79. The method of Claim 66 wherein said crystal oscillator is an external crystal oscillator (XOSC).

80. The method of Claim 66 wherein said crystal oscillator includes an external crystal and an amplifier and further comprising integrating said amplifier with one of said MAC device, said BB processor, and said RF transceiver.

81. The method of Claim 61 wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle.

82. The method of Claim 61 wherein said wireless Ethernet network device dissipates less than 2mW when in said low power mode.

83. The method of Claim 66 further comprising calibrating said first oscillator using said timing signal from said crystal oscillator.

84. The method of Claim 68 further comprising locating said first oscillator in said BB processor.

85. The method of Claim 68 further comprising implementing at least two of said BB processor, said first voltage regulator, said second voltage regulator, said RF transceiver, said MAC device, and said first PLL using a system on chip (SOC).

86. A method for operating a baseband processor for a wireless Ethernet network device with active and low power modes, comprising:

regulating supply voltage using a first voltage regulator during the active mode;

powering down the first voltage regulator during the low power mode; and

regulating supply voltage using a second voltage regulator, which dissipates less power than said first voltage regulator, during the low power mode.

87. The method of Claim 86 further comprising receiving a power mode select signal from a medium access controller.

88. The method of Claim 86 further comprising:

generating a first clock signal using a first PLL during the active mode; and

powering down the first PLL during the low power mode.

89. The method of Claim 88 wherein said first PLL receives a timing signal from a crystal oscillator during the active mode.

90. The method of Claim 89 further comprising generating a second clock signal during the low power mode using a first oscillator that dissipates less power than the crystal oscillator.